WHAT IS CLAIMED IS:

1. A method for refreshing dynamic memory cells arranged along word lines and bit lines, comprising:

generating a refresh signal to activate a word line to refresh a charge stored in memory cells arranged on the word line;

monitoring an amount of charge loss of one or more sets of dynamic reference cells; and

adjusting a frequency of the refresh signal based on the monitored amount of charge loss.

2. The method of claim 1, wherein the frequency of the refresh signal is set by dividing a fundamental frequency by a frequency divider.

3. The method of claim 2, wherein adjusting the frequency of the refresh signal comprises adjusting the frequency divider.

4. The method of claim 3, wherein adjusting the frequency divider comprises:

increasing the frequency divider if the monitored amount of charge loss falls below a first threshold value; and

decreasing the frequency divider if the monitored amount of charge loss exceeds a second threshold value.

5. The method of claim 4, wherein the first and second threshold values are different.

6. The method of claim 1, wherein monitoring the amount of charge loss of the one or more sets of reference cells comprises:

precharging a first set of the reference cells on a first reference word line to a first potential value;

isolating the first set of reference cells from a first common bit line;

a known time later, connecting the first set of reference cells to the first common bit line; and

comparing a potential on the first common bit line with a first reference potential.

7. The method of claim 6, further comprising precharging the first common bit line to a center potential.

8. The method of claim 6, wherein the first reference potential is a ground reference.

9. The method of claim 6, further comprising:

precharging a second set of the reference cells on a second reference word line to a second potential value;

isolating the second set of reference cells from a second common bit line;

a known time later, connecting the second set of reference cells to the second common bit line; and

comparing a potential on the second common bit line with a second reference potential.

10. The method of claim 9, wherein adjusting the frequency of the refresh signal based on the monitored amount of charge loss comprises:

increasing the frequency of the refresh signal if the potential on the first common bit line exceeds the first reference potential or the second reference potential exceeds the potential on the second common bit line; and

decreasing the frequency of the refresh signal if the first reference potential exceeds the potential on the first common bit line and the potential on the second common bit line exceeds the second reference potential.

11. A circuit for adjusting a frequency of a refresh signal used to refresh dynamic memory cells, comprising:

a first set of reference cells connectable to a first common bit line by activation of a first common word line;

a second set of reference cells connectable to a second common bit line by activation of a second common word line; and

a regulating unit configured to monitor an amount of charge loss of the first and second reference cells and adjust the frequency of the refresh signal used to refresh the dynamic memory cells based on the monitored amount of charge loss.

12. The circuit of claim 11, wherein the regulating unit is configured to generate one or more control signals to activate the first and second sets of reference cells in order to monitor the amount of charge loss of the first and second reference cells.

13. The circuit of claim 11, wherein the regulating unit is configured to:

increase the frequency of the refresh signal if the loss of charge of either the first and second sets of reference cells exceeds a threshold amount; and

decrease the frequency of the refresh signal if the loss of charge of both the first and second sets of reference cells does not exceed the threshold amount.

14. The circuit of claim 11, wherein the regulating circuit is configured to:

precharge the first and second sets of reference cells to respective first and second potential values;

isolating the first and sets of reference cells from the respective first and second common bit lines;

a known time later, connect the first and second sets of reference cells to the respective first and second common bit lines;

determine the charge loss of the first set of reference cells by comparing a potential on the first common bit line with a first reference potential; and

determine the charge loss of the second set of reference cells by comparing a potential on the second common bit line with a second reference potential.

15. The circuit of claim 14, wherein:

the first potential value is ground;

the second potential value is above ground;

the regulating unit is configured to increase the frequency of the refresh signal if the potential on the first common bit line exceeds the first reference potential, the second reference potential exceeds the potential on the second common bit line, or both; and

the regulating unit is configured to decrease the frequency of the refresh signal if the first reference potential exceeds the potential on the first common bit line and the potential on the second common bit line exceeds the second reference potential.

16. The circuit of claim 14, wherein the regulating circuit is configured to precharge the first and second common bit lines to a center potential prior to connecting the first and second sets of reference cells to the respective first and second common bit lines.

17. The circuit of claim 11, wherein the regulating unit initiates the monitoring of charge loss of the first and second sets of reference cells and the adjusting of the frequency of the refresh signal based on one or more word address signals received from a refresh circuit.

18. A memory device, comprising:

a plurality of dynamic memory cells arranged along word lines and bit lines of the device;

at least a first set of reference cells arranged around a first common word line and a first common bit line;

a refresh circuit for generating a refresh signal to refresh the dynamic memory cells; and

a refresh frequency adjust circuit to adjust a frequency of the refresh signal based on a monitored amount of charge loss of the first set of reference cells.

19. The memory device of claim 18, wherein:

a frequency of the refresh signal is established by dividing a fundamental frequency of an oscillator circuit by a counter value; and

the refresh frequency adjust circuit is configured to adjust the frequency of the refresh signal by adjusting the counter value.

20. The memory device of claim 18, further comprising:

at least a second set of reference cells arranged around a second common word line and a second common bit line; and

wherein the refresh frequency adjust circuit is configured to adjust the frequency of the refresh signal based on a monitored amount of charge loss of both the first and second sets of reference cells.